TERMINAL LEARNING OBJECTIVE

ACTION

Troubleshoot the five basic digital flip-flops.

CONDITION

Given a classroom environment, Computer Aided Instruction (CAI) workstation, NIDA 130 Electronic Trainer, Digital Multimeter w/test leads, Digital Logic Probe, PC130-111, PC130-113, PC130-115, and official OMEMS reference material.

STANDARD

Correctly answer 18 of 25 questions concerning the five basic digital flip-flops.

CLASSIFICATION:	**UNCLASSFIED**
SAFETY CONSIDERATIONS:	**ELECTRICAL SHOCK HAZARD**
	ELECTOSTATIC DISCHARGE
ENVIRONMENTAL:	**NONE**
RISK ASSESMENT:	**LOW**

ENABLING LEARNING OBJECTIVE 1

ACTION

Define Digital Flip-Flops, describe the operation of the Reset-Set flip-flop, construct a truth table and timing chart for Reset-Set flip-flop.

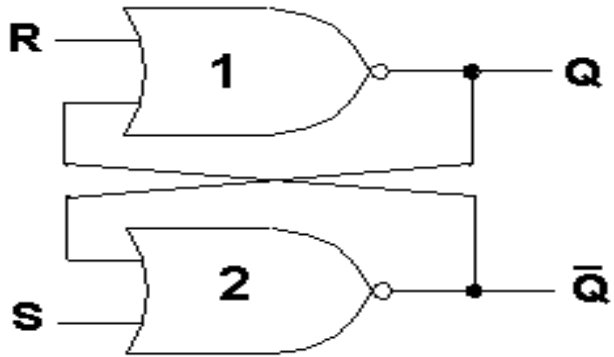
CONDITION

Given a classroom environment, Computer Aided Instruction (CAI) workstation, NIDA 130 Electronic Trainer, Digital Multimeter w/test leads, Digital Logic Probe, PC130-111, PC130-113, PC130-115, and official OMEMS reference material.

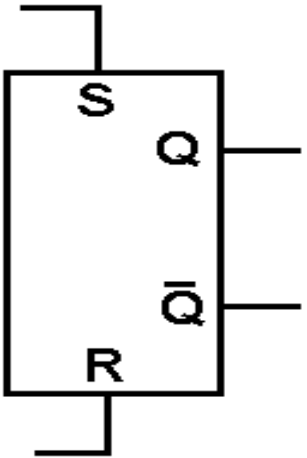
STANDARD

Correctly answer 18 of 25 questions concerning the five basic digital flip-flops

FLIP-FLOPS are temporary storage devices having two steady states. The circuit normally remains in one state until a pulse is applied to the input of the circuit, causing it to switch to the other state.



Active-High Input Reset-Set Flip-Flop

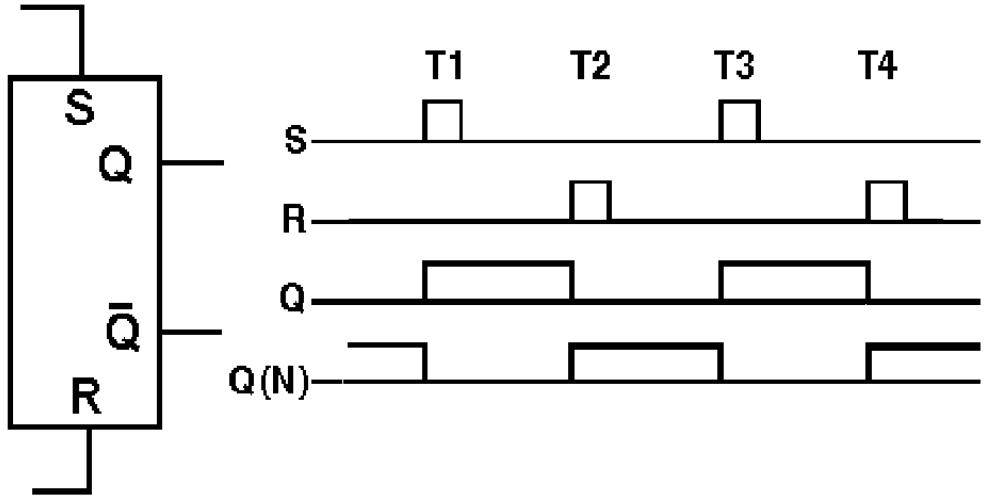


Graphic Symbol Active-High RS Flip-Flop

4-400-11

Inputs		Outputs		
S	R	Q	$\bar{Q}$	Comments
0	0	NC	NC	*No change*
0	1	0	1	*Latch Resets*
1	0	1	0	*Latch Sets*
1	1	1	1	*Invalid condition*

Active-High RS Truth Table



Active-High RS Flip-Flop And Timing Diagram

How can you tell if a flip-flop is HIGH active or LOW active?

1. The symbol has a 1 or 0 on it.
2. + or - on the input and output.
3. Bubbles indicate HIGH active and without bubbles indicate a LOW active.
4. Bubbles indicate LOW active and without bubbles indicate HIGH active.

Flip-Flops are temporary storage devices having two steady states. The circuit normally stores the last input condition until the last input is fed back.

1. TRUE

2. FALSE

What is the output of a High input activated RS flip-flop when both the S and R inputs go high at the same time ?

1. Unable to determine
2. Q HIGH, Q[N] LOW
3. Q LOW, Q[N] HIGH
4. Q and Q[N] HIGH

ENABLING LEARNING OBJECTIVE 2

ACTION

Define Synchronous Flip-Flops, describe the operation of the clocked Reset-Set flip-flop, construct a truth table and timing diagram, and variations for a clocked Reset-Set flip-flop.

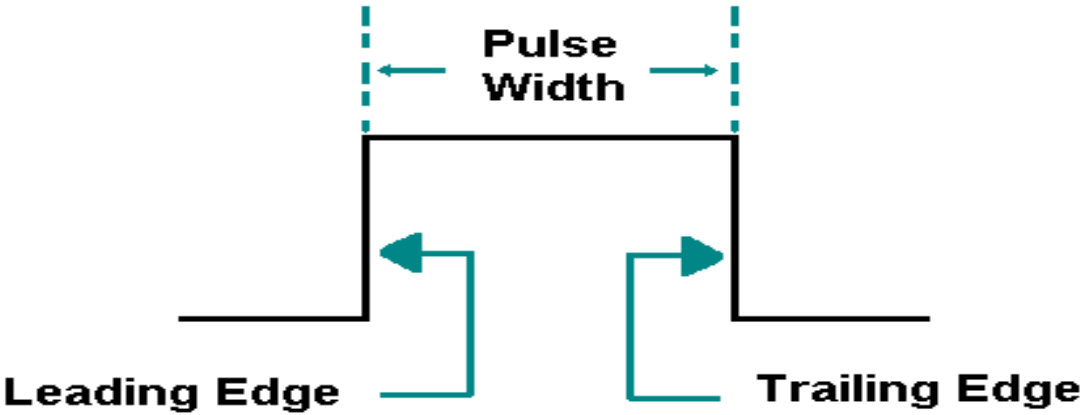
CONDITION

Given a classroom environment, Computer Aided Instruction (CAI) workstation, NIDA 130 Electronic Trainer, Digital Multimeter w/test leads, Digital Logic Probe, PC130-111, PC130-113, PC130-115, and official OMEMS reference material.

STANDARD

Correctly answer 18 of 25 questions concerning the five basic digital flip-flops

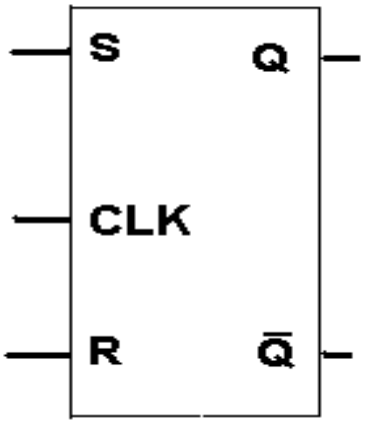
SYNCHRONOUS FLIP-FLOPS

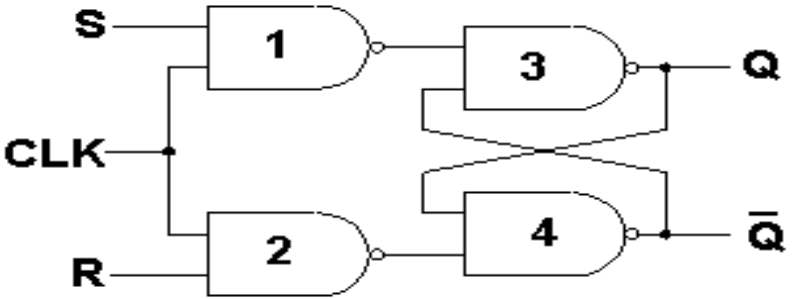


Clock Triggering

4-400-12

FLIP-FLOP TRIGGERING	
Level triggered	uses high or low pulse width
Edge triggered	uses leading or trailing edge
Pulse triggered	uses high and low (level) or leading and trailing (edge)

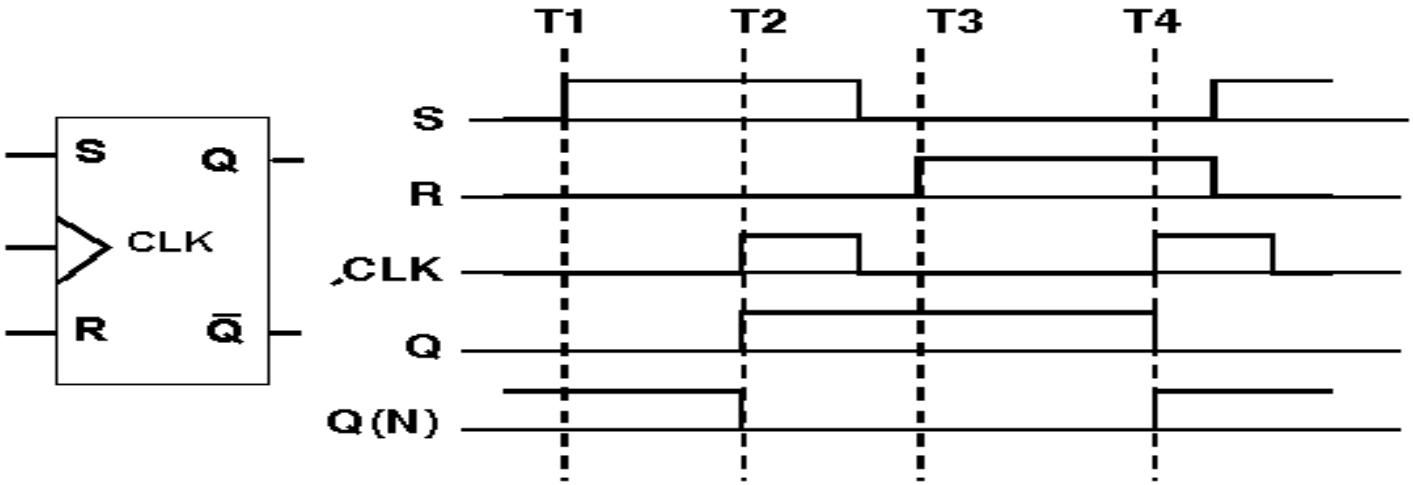




Active-High Clocked RS Flip-Flop

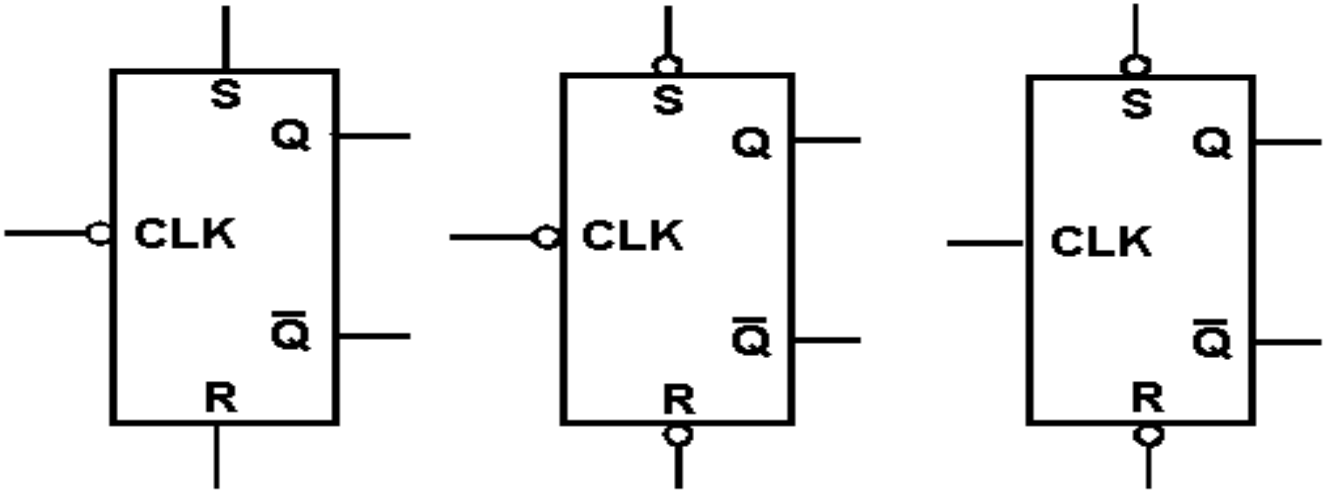
Inputs			*Outputs*		
S	**R**	**CLK**	**Q**	$\bar{Q}$	*Comments*
0	0	X	NC	NC	*No change*
0	1	1	0	1	*Latch Resets*
1	0	1	1	0	*Latch Sets*
1	1	1	?	?	*Invalid condition*

Active-High Clocked RS Truth Table



Active-High Clocked RS Flip-Flop And Timing Diagram

4-405-04



Clocked RS Flip-Flop Variations

Why is a clocked RS flip-flop considered a synchronous circuit ?

1. Because the output can change only with the command of a clock signal.
2. Because the Q and Q[N] signals change together.
3. Because the R and S inputs are opposites for normal operation.
4. Because the set and reset signals are not applied at the same time.

High applied to the S input of a high activated clocked RS flip-flop

1. sets Q HIGH and Q[N] LOW.
2. sets Q LOW and Q[N] HIGH.
3. will not set Q High unless CLK is LOW.
4. will not set Q HIGH unless CLK is HIGH.

ENABLING LEARNING OBJECTIVE 3

ACTION

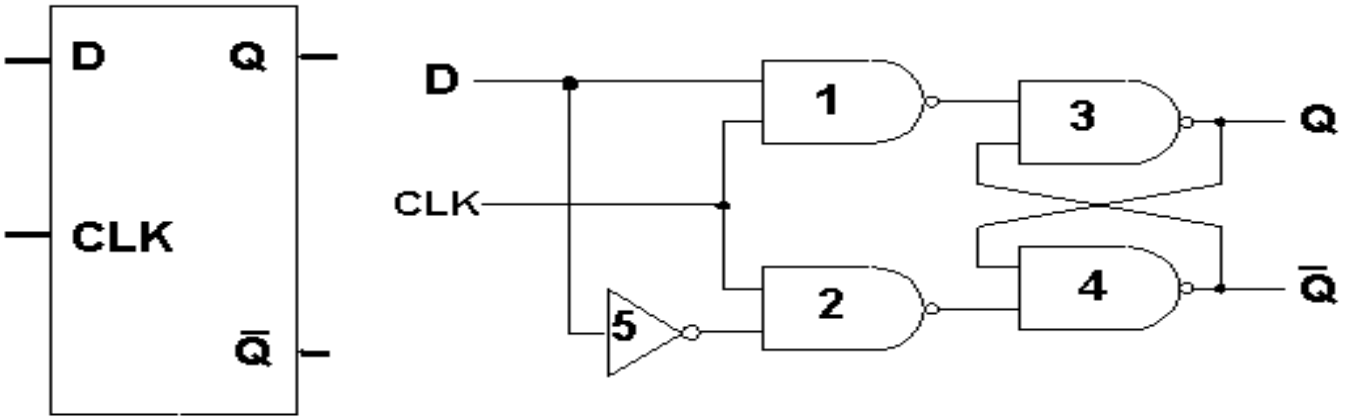
Describe the operation of the D type flip-flop, construct a truth table and timing diagram, and variations for a D type flip-flop.

CONDITION

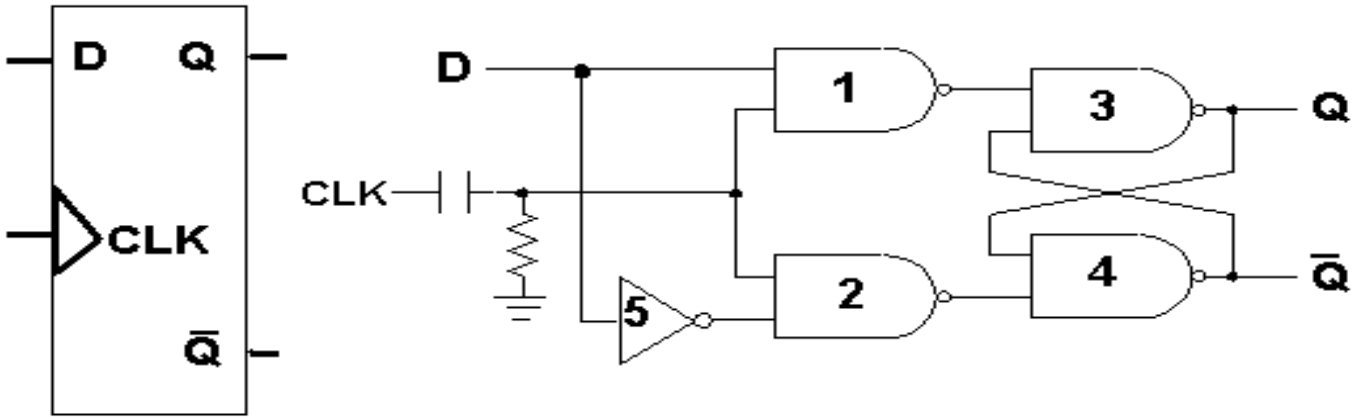
Given a classroom environment, Computer Aided Instruction (CAI) workstation, NIDA 130 Electronic Trainer, Digital Multimeter w/test leads, Digital Logic Probe, PC130-111, PC130-113, PC130-115, and official OMEMS reference material.

STANDARD

Correctly answer 18 of 25 questions concerning the five basic digital flip-flops



High Gated D Type Flip-Flop

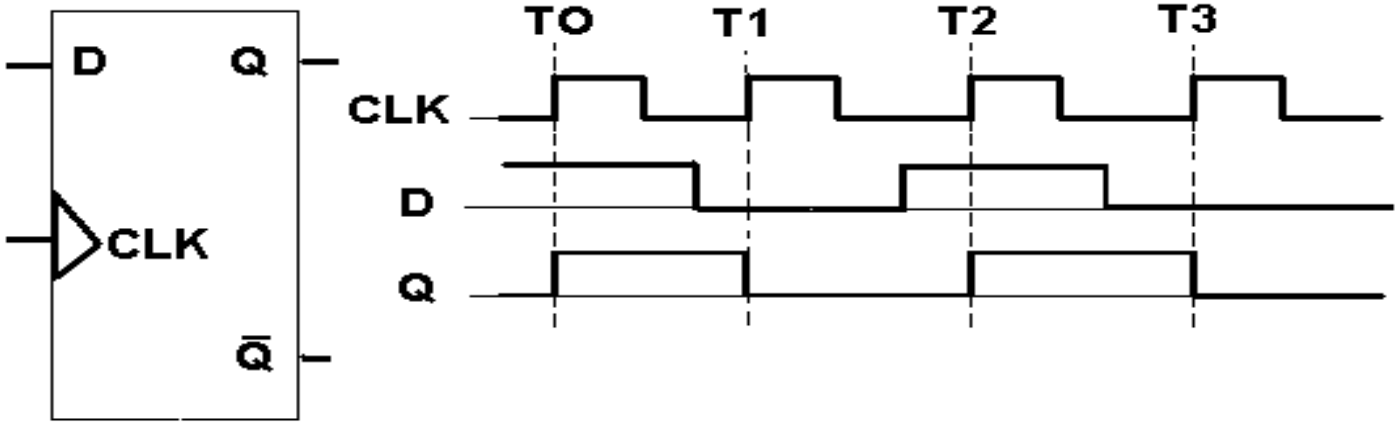


Edge Triggered D Type Flip-Flop

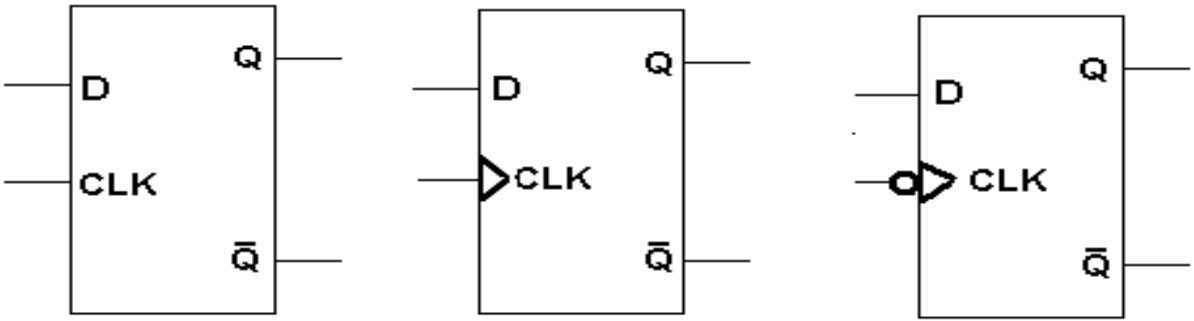
Inputs		*Outputs*		
D	**CLK**	**Q**	**$\bar{Q}$**	*Comments*
1	**L - H**	**1**	**0**	**Flip-Flop Set**
0	**L - H**	**0**	**1**	**Flip-Flop Reset**

Edge Triggered D Type Flip-Flop
Truth Table

ELEC-S16



Edge Triggered D Type Flip-flop Timing Diagram



D Type Flip-Flop Variations

When the Clock input changes a D type flip-flop, what does the Q output do ?

1. Goes opposite of D
2. Nothing
3. Follow the Q[N]
4. Follow the D input

What does the small triangle on the clock input of a D type flip-flop schematic symbol indicate ?

1. It is a D latch
2. Requires a HIGH CLK input
3. Requires a LOW CLK input
4. Is an edge triggered device

ENABLING LEARNING OBJECTIVE 4

ACTION

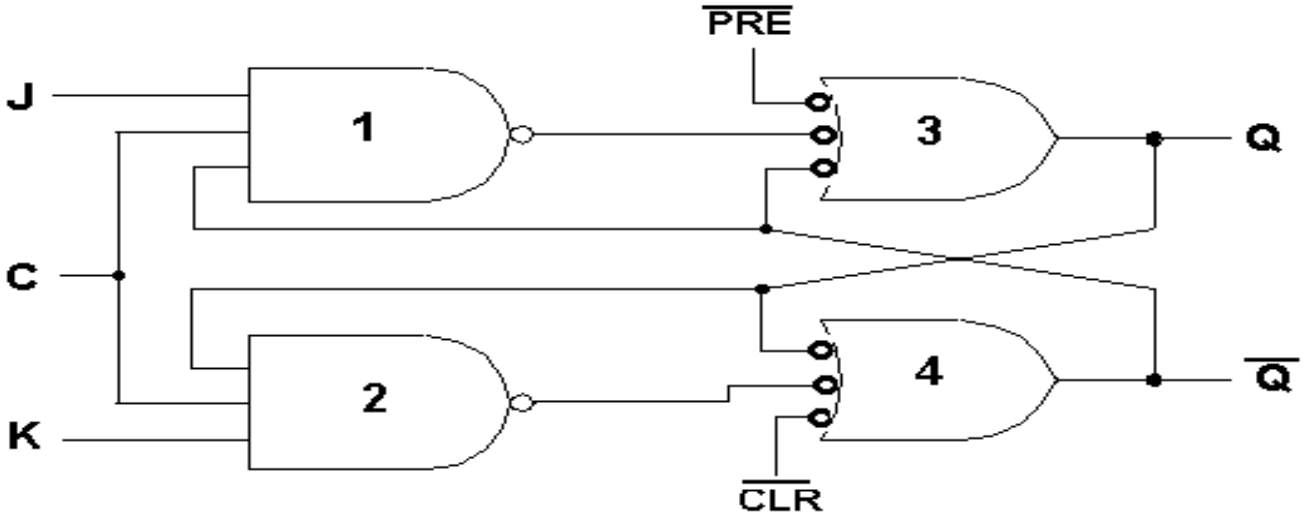
Describe the operation of the JK flip-flop, construct a truth table and timing diagram for a JK type flip-flop.

CONDITION

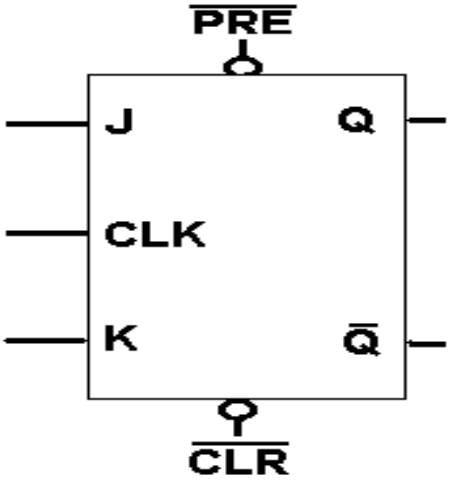
Given a classroom environment, Computer Aided Instruction (CAI) workstation, NIDA 130 Electronic Trainer, Digital Multimeter w/test leads, Digital Logic Probe, PC130-111, PC130-113, PC130-115, and official OMEMS reference material.

STANDARD

Correctly answer 18 of 25 questions concerning the five basic digital flip-flops

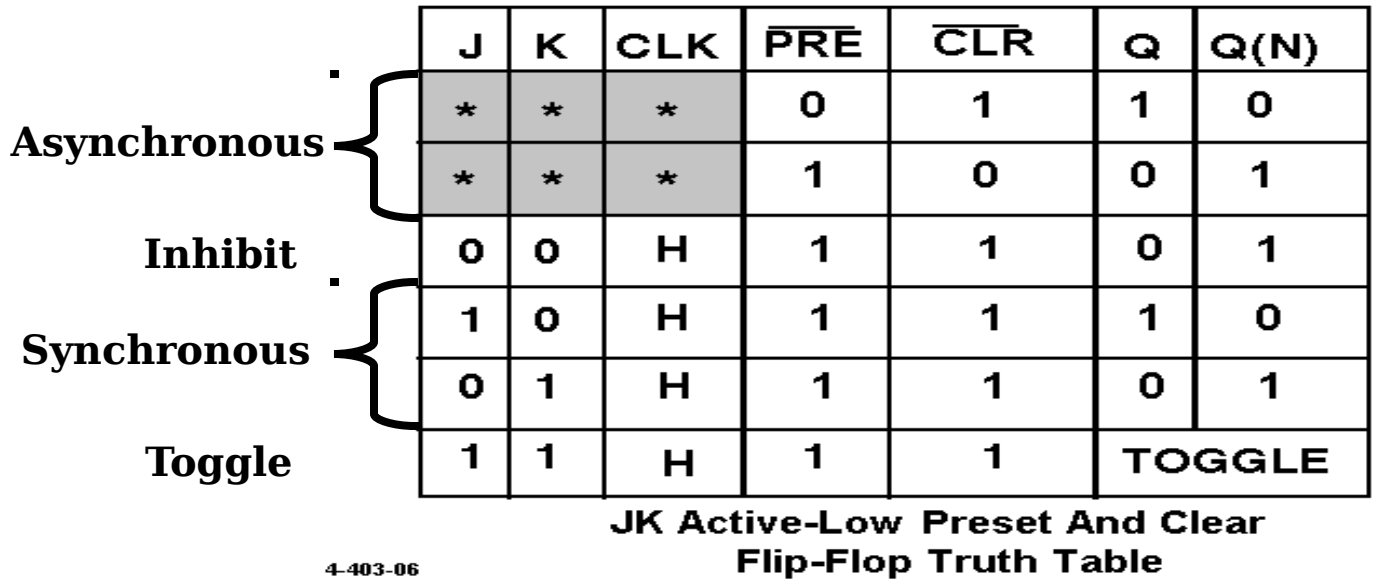


JK Active-Low Preset And Clear Flip-Flop

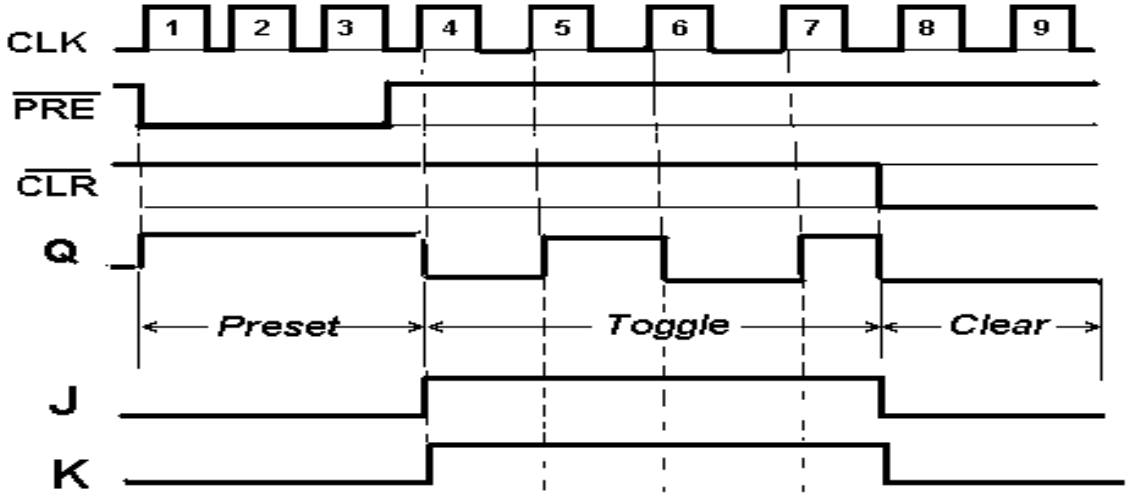


Graphic Symbol JK Flip-Flop

4.403.01



JK Active-Low Preset And Clear Flip-Flop Truth Table



JK Active-Low Preset And Clear Flip-Flop Timing Diagram

4-403-07

What is the operation of a JK flip-flop called when the J and K inputs are held low ?

1. Toggle
2. Asynchronous
3. Inhibit
4. Synchronous

Which JK flip-flop input has precedence over all others ?

1. J
2. K
3. CLOCK
4. CLEAR

ENABLING LEARNING OBJECTIVE 5

ACTION

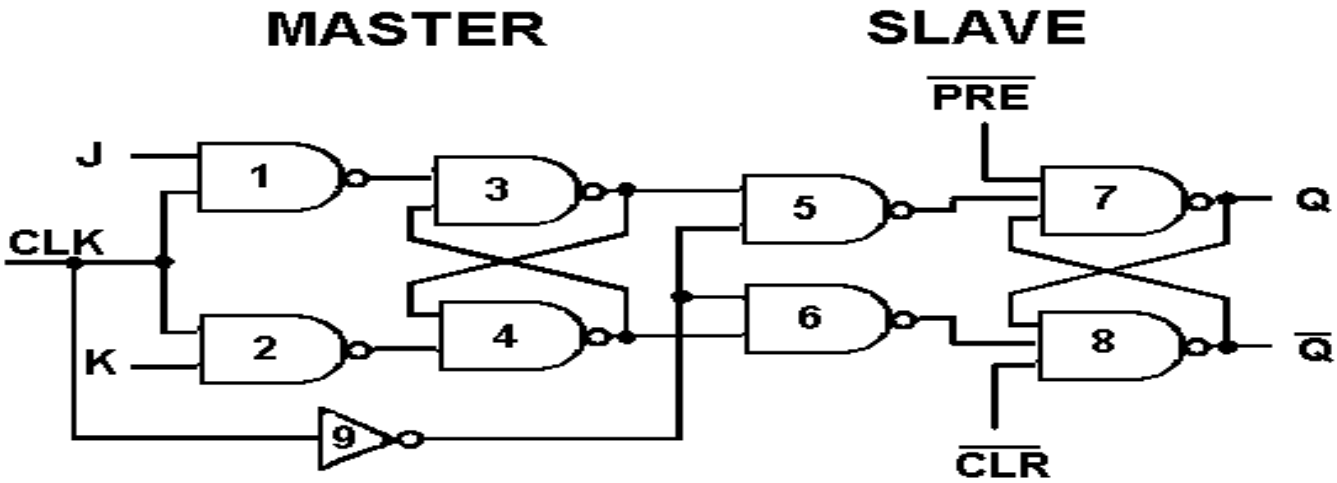
Describe the operation of the Master Slave flip-flop, discuss the clock pulse and logic symbol for the Master Slave flip-flop.

CONDITION

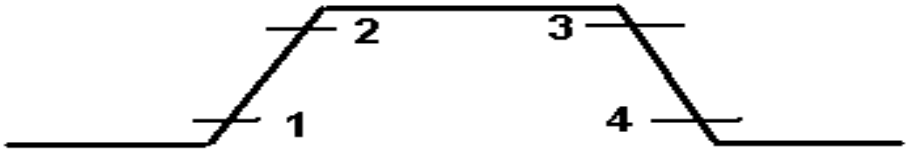
Given a classroom environment, Computer Aided Instruction (CAI) workstation, NIDA 130 Electronic Trainer, Digital Multimeter w/test leads, Digital Logic Probe, PC130-111, PC130-113, PC130-115, and official OMEMS reference material.

STANDARD

Correctly answer 18 of 25 questions concerning the five basic digital flip-flops



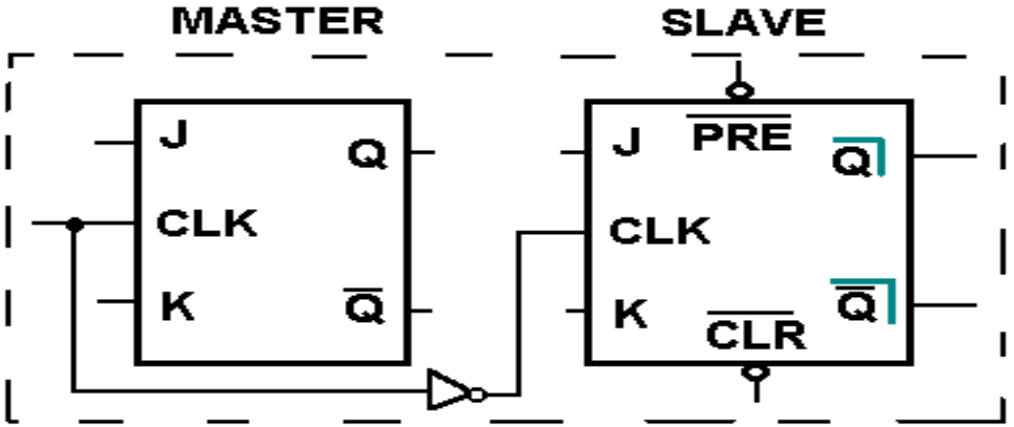
Master Slave J-K Flip-Flop



Point 1:	***Clock pulse starts positive, master and slave are isolated.***
Point 2:	***J and K inputs transfered into master.***
Point 3:	***J and K inputs stored into master.***
Point 4:	***J and K outputs transferred to slave.***

J-K Master Slave Gated Clock Pulse

4-497-04



Graphic Symbol Master Slave Flip-flop

What type of triggering is used by a master slave flip-flop ?

1. LEVEL
2. CLOCK
3. EDGE
4. PULSE

ENABLING LEARNING OBJECTIVE 6

ACTION

Complete CAI lessons on the Reset-Set flip flop, the Clocked Reset-Set flip flop, the D-type flip flop, the J-K flip flop, and the Master-Slave flip flop.

CONDITION

Given a classroom environment, Computer Aided Instruction (CAI) workstation, NIDA 130 Electronic Trainer, Digital Multimeter w/test leads, Digital Logic Probe, PC130-111, PC130-113, PC130-115, and official OMEMS reference material.

STANDARD

Correctly answer 18 of 25 questions concerning the five basic digital flip-flops

ENABLING LEARNING OBJECTIVE 7

ACTION

Perform troubleshooting procedures on the Reset-Set flip flop, the Clocked Reset-Set flip flop, the D-type flip flop, the J-K flip flop, and the Master-Slave flip flop.

CONDITION

Given a classroom environment, Computer Aided Instruction (CAI) workstation, NIDA 130 Electronic Trainer, Digital Multimeter w/test leads, Digital Logic Probe, PC130-111, PC130-113, PC130-115, and official OMEMS reference material.

STANDARD

Correctly identify 10 of 10 malfunctions in the Reset-Set flip flop, the Clocked Reset-Set flip flop, the D-type flip flop, the J-K flip flop, and the Master-Slave flip flop.